Performance Counters

Libmsr Version 0.2.1

There are performance counters in many domains supported by LIBMSR.

- The fixed performance counters always count a single event, there is one for instructions retired, unhalted core cycles, and unhalted reference cycles.
- The architectural counters are the same accross all architectures since their creation. You can program the event you want them to count into another register.
- The uncore counters typically change between architectures. Most of them are for the "Cbo" or caching agent. See the uncore performance guide of your architecture for more details.

Fixed Counters

1. Call enable_fixed_counters()
2. Use the dump functions to print the data, or use the storage function to access the raw MSR data.

Architectural Counters

> These counters are programmable, meaning you can indicate what performance event you want them to count. To find this information see Intel Architectures Software Developer Manual sections 18 and 19.

1. Set the event for a counter with either set_pmc_ctrl (single thread) or set_all_pmc_ctrl (all threads). Note that you must figure out the correct flags (once again see the documentation).
2. call enable_pmc to have settings go into effect
3. use a dump function to print results out or a storage function if you need raw data

```
// Count all branch instructions retired (0xC4)

// for all rings and enable the counter (0x67) on pmc1 and pmc2
set_all_pmc_ctrl(0x0, 0x67, 0x0, 0xC4, 1);
set_all_pmc_ctrl(0x0, 0x67, 0x0, 0xC4, 2);
enable_pmc();
dump_pmc_readable();
```

Uncore Counters

To be completed...

Related articles

- PCI Configuration Registers (CSRs)
- The Batch Interface
- RAPL
- Performance Counters
- General LIBMSR Use